

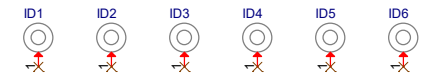
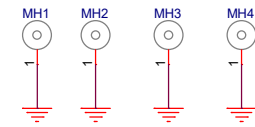
8MM Base

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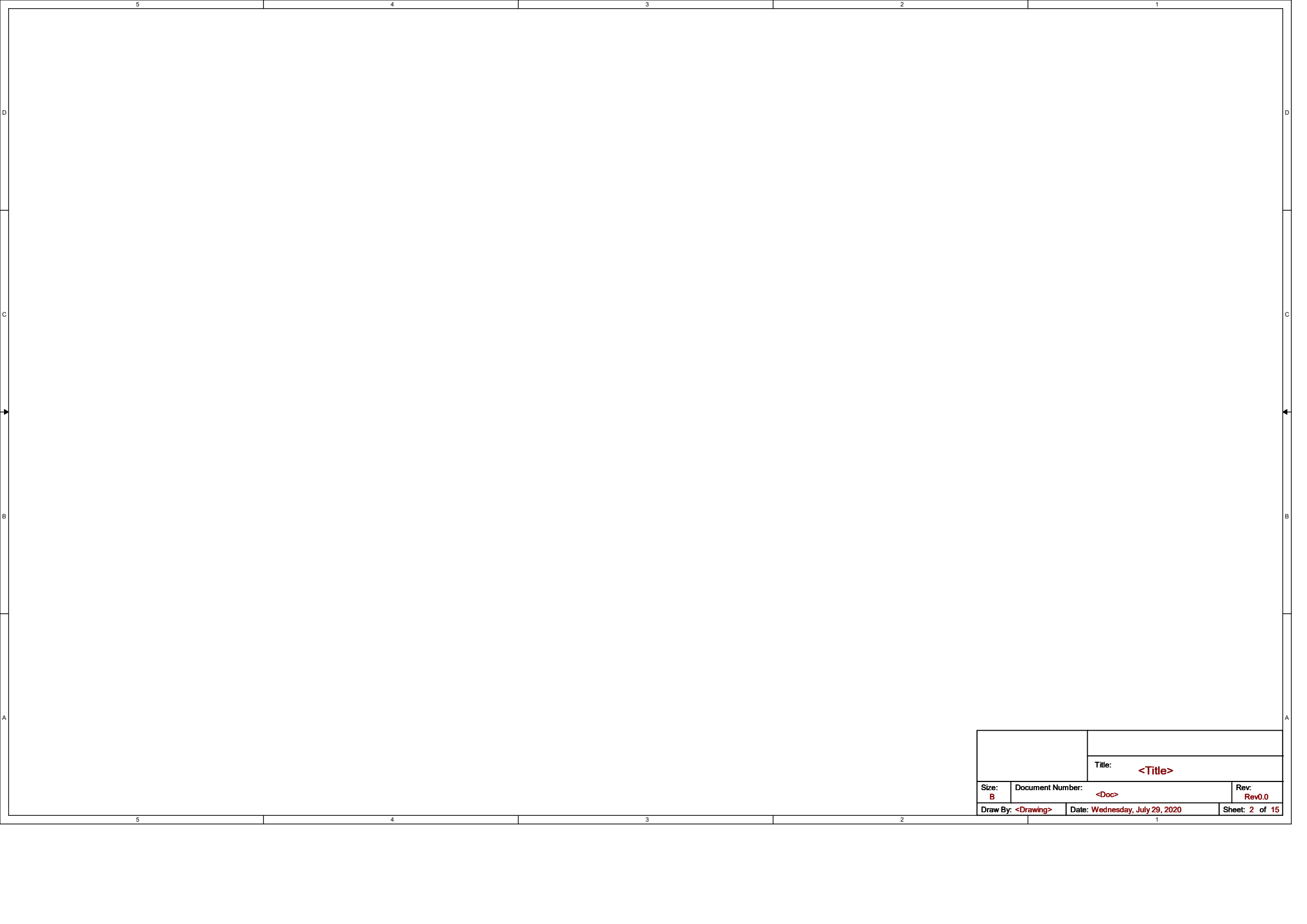
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Revision History

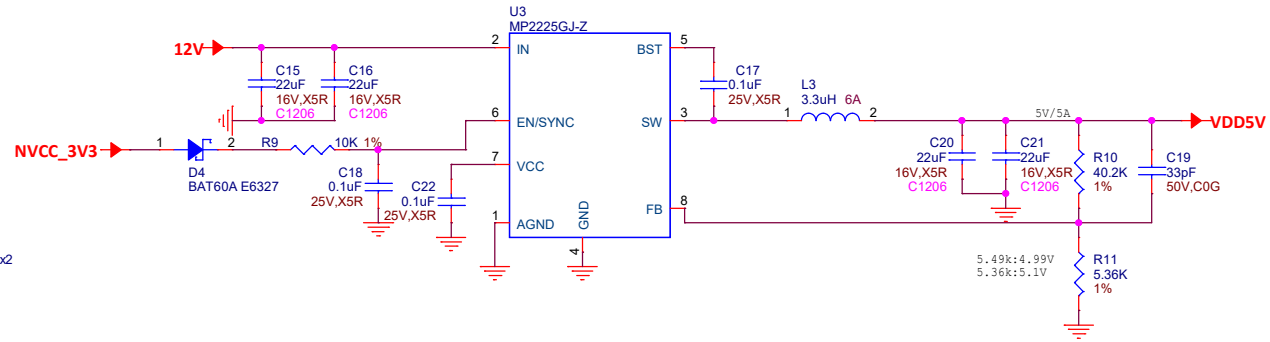
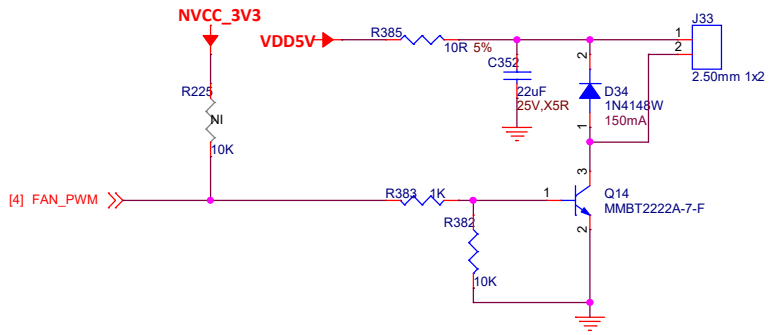
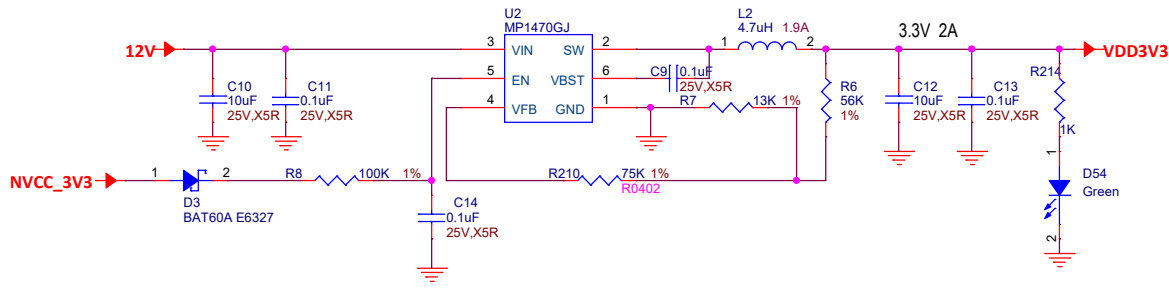
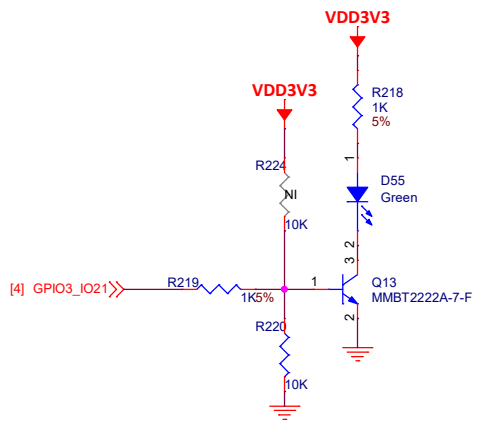
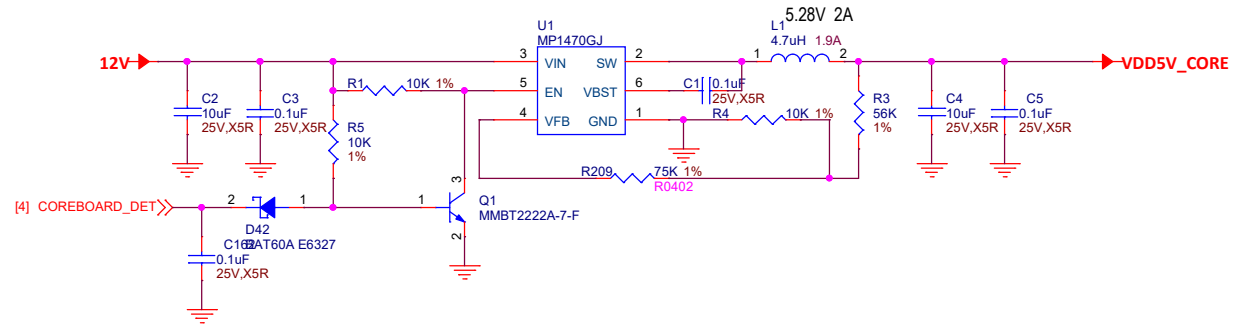
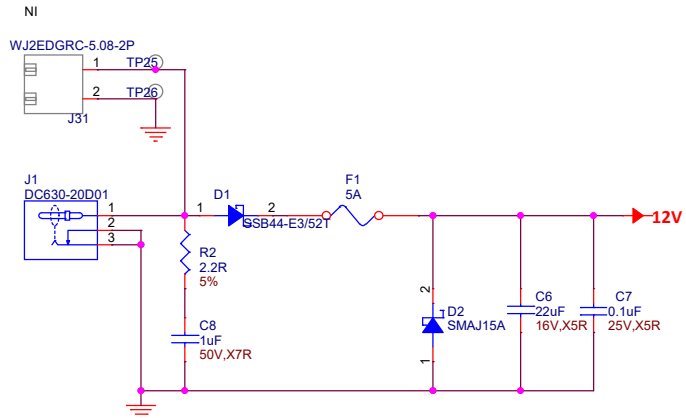
Rev. Code	Date	By	Description
Rev:00	2018-11-30	Jake	First version



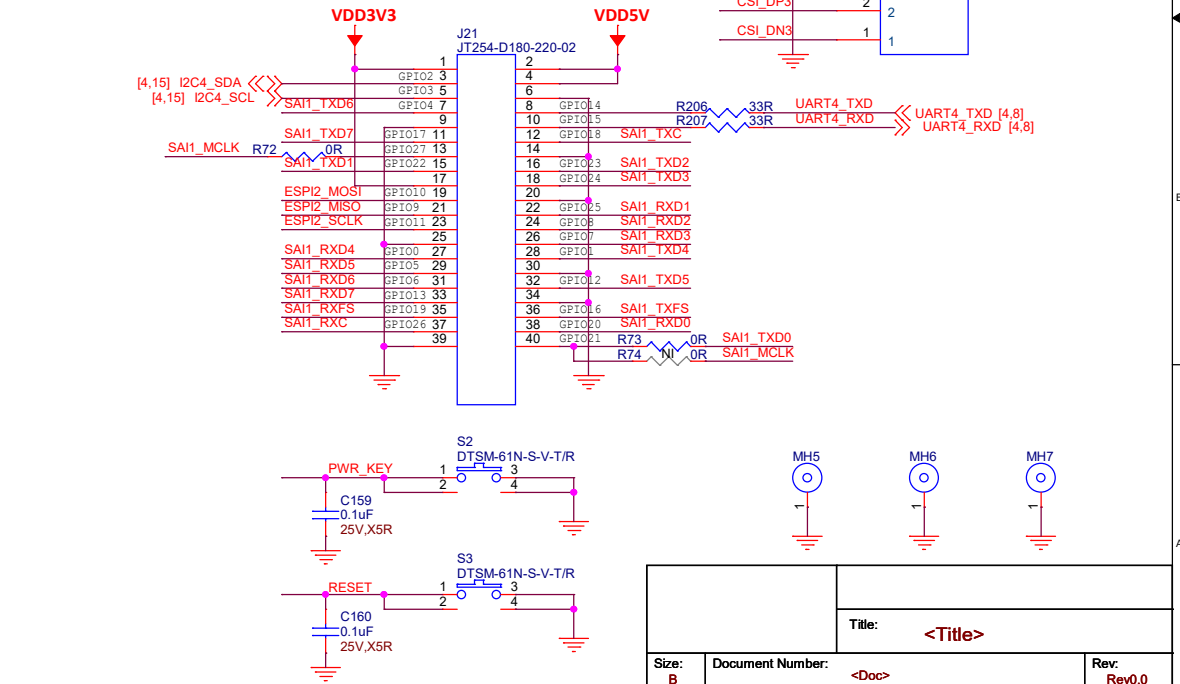
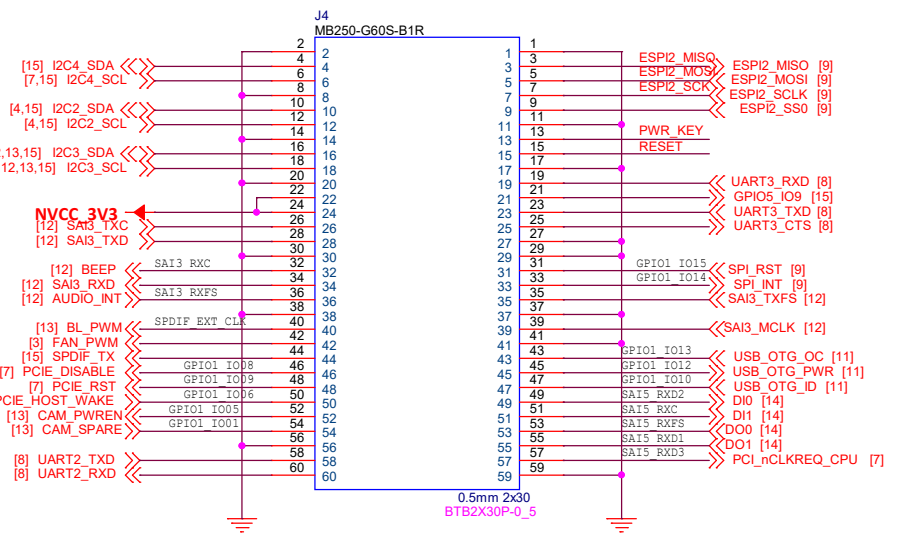
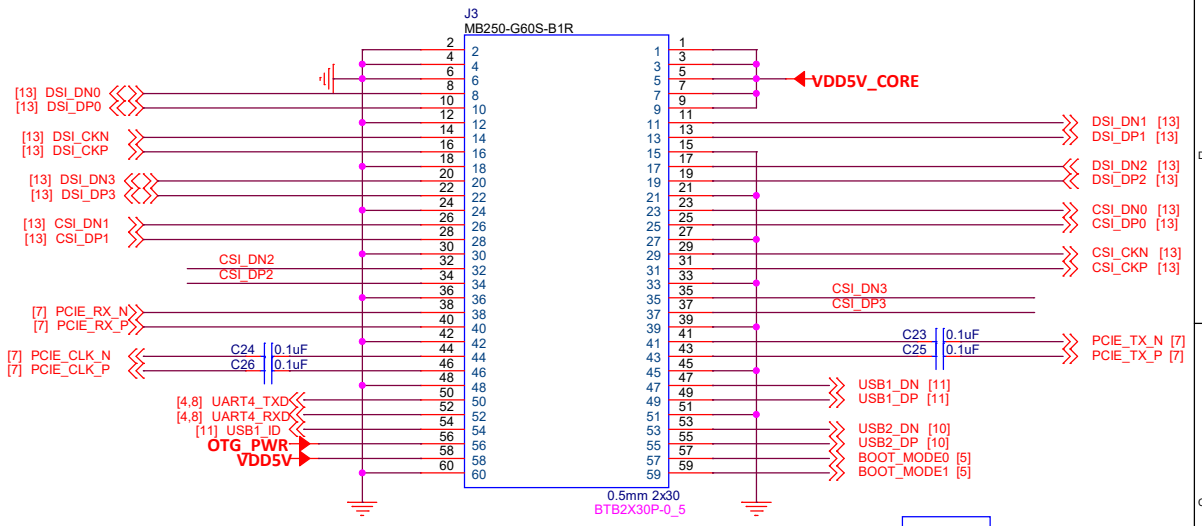
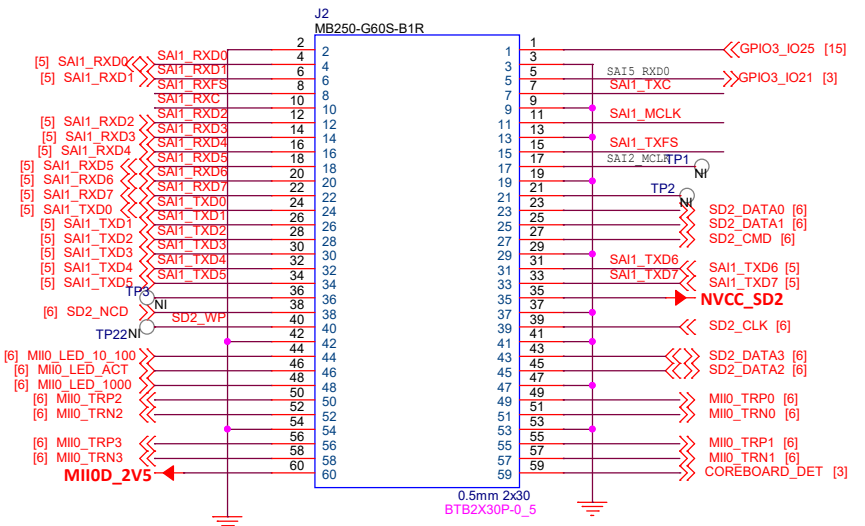
		Title: <Title>	
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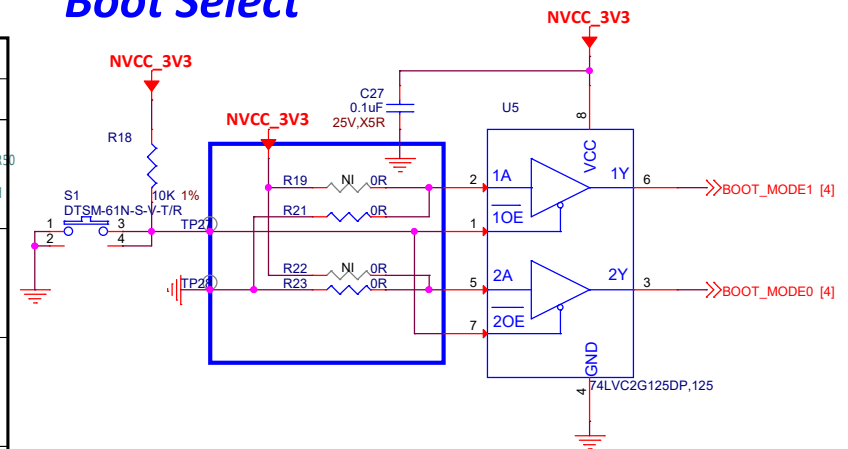


Title: <Title>	
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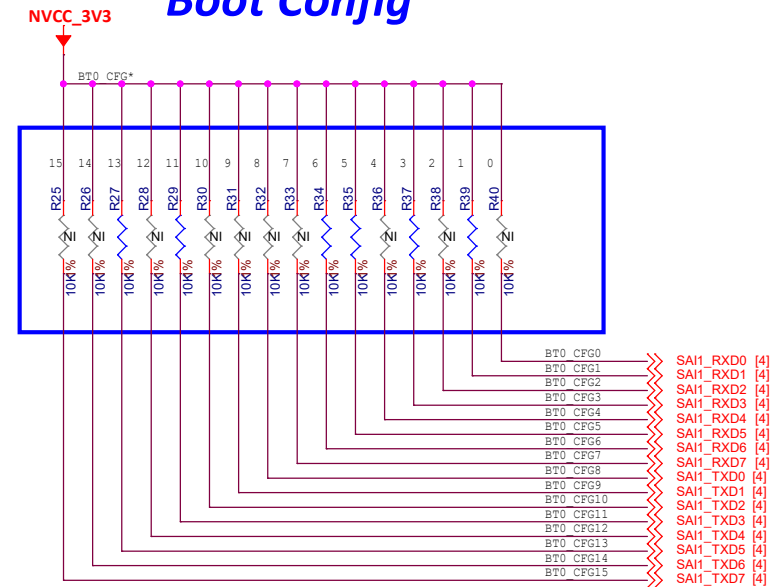
i.MX8M Mini ROM Fuse

Address	7	6	5	4	3	2	1	0	
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	Infini-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD		Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via		SD Loopback Clock Source Sel (for SDR30 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND		Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5		
	0x470[15:8]		100 - QSPI		Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			
	0x470[15:8]		110 - SPI NOR		Port Select: 000 - eCSP1 001 - eCSP2 010 - eCSP3		SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)		
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - FastBoot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.	Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V		USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V	
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz: Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.			Reserved	
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Boot Select

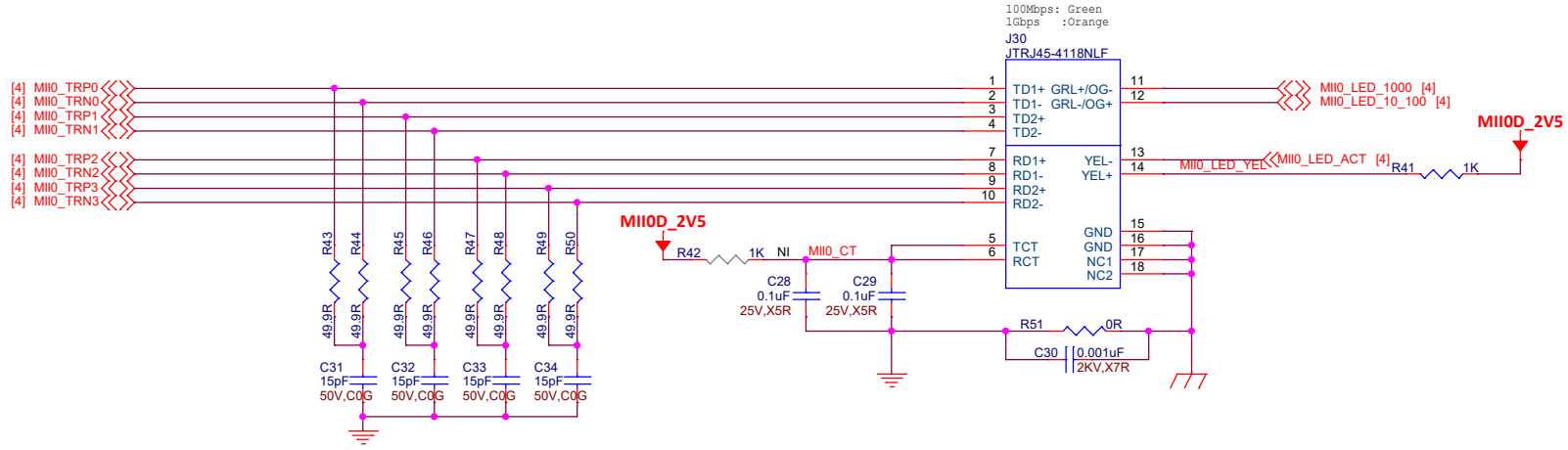


Boot Config

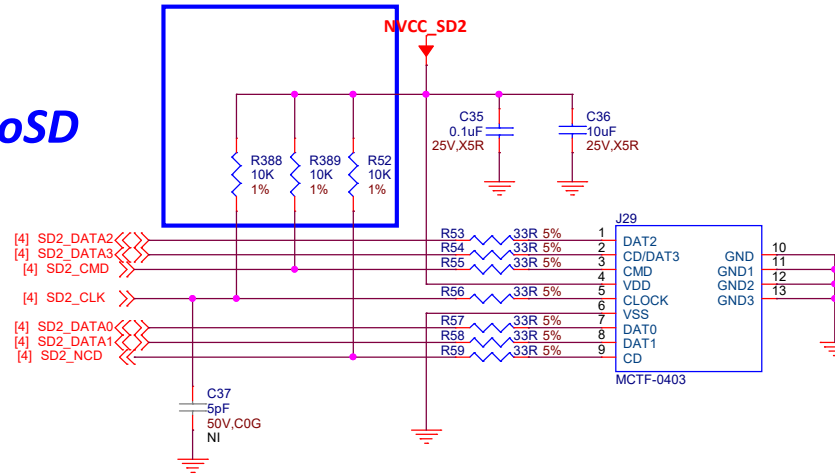


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Ethernet

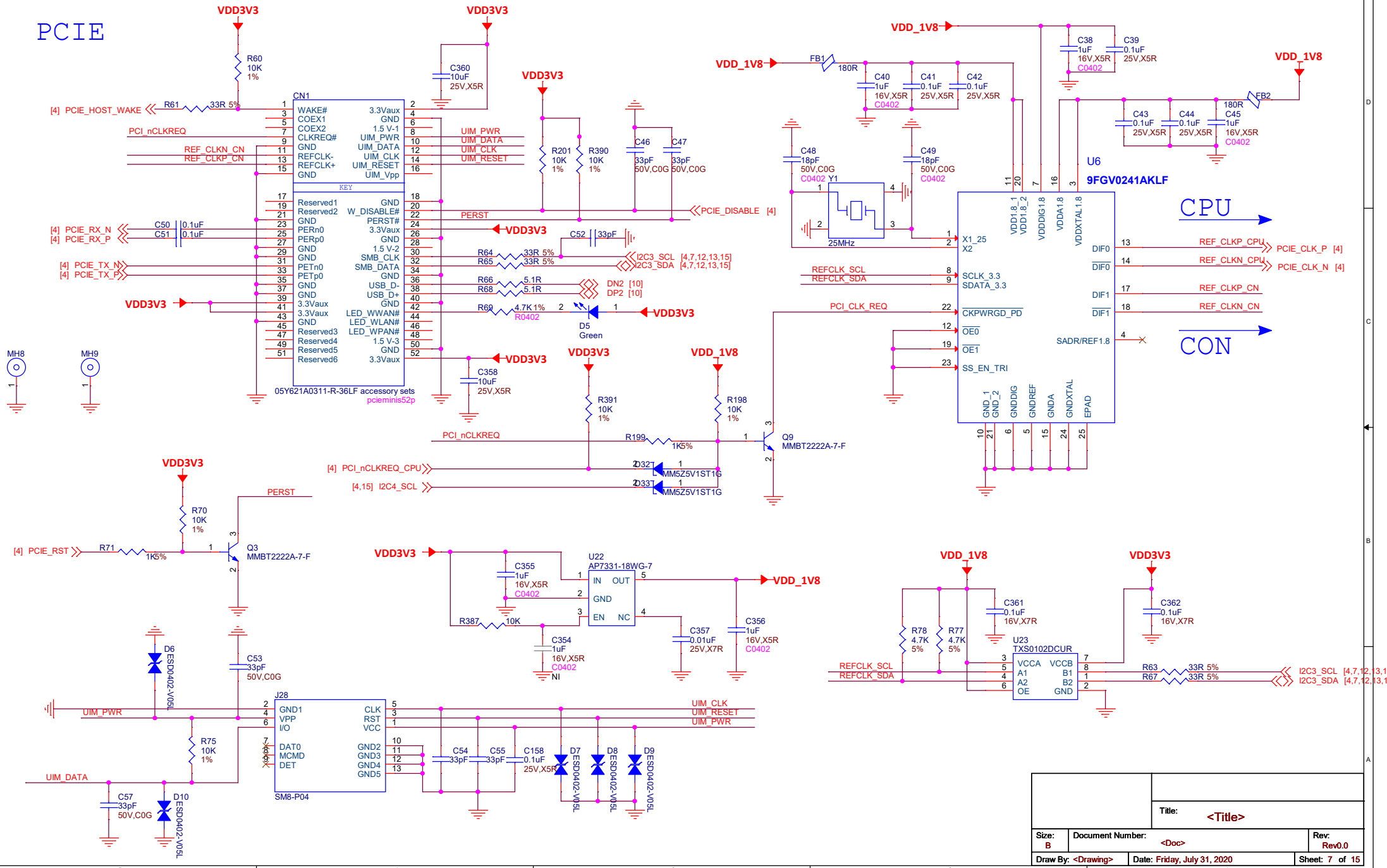


MicroSD

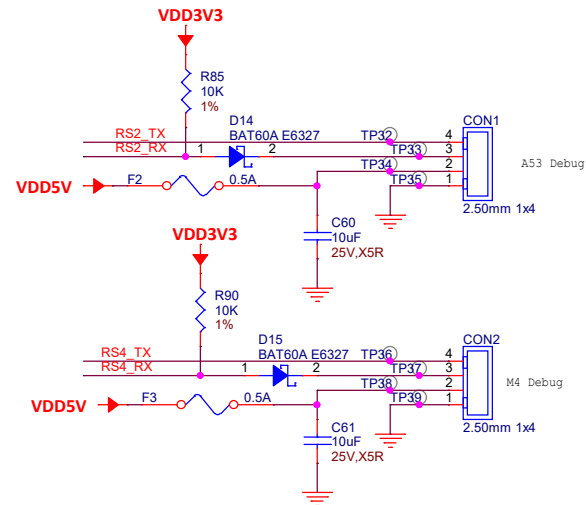
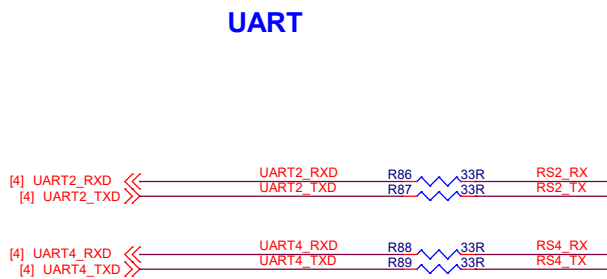
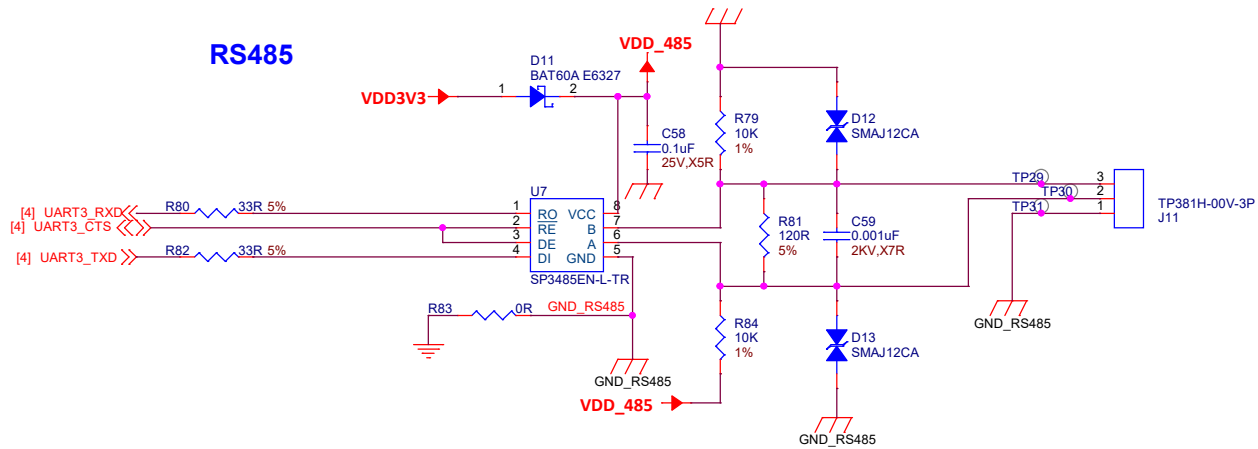


Title: <Title>	
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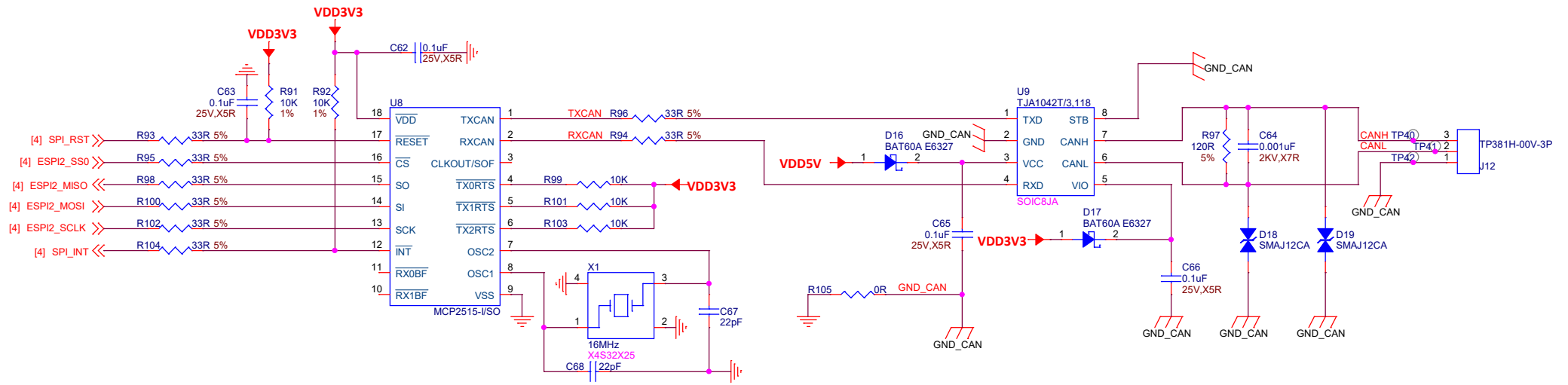
PCIE



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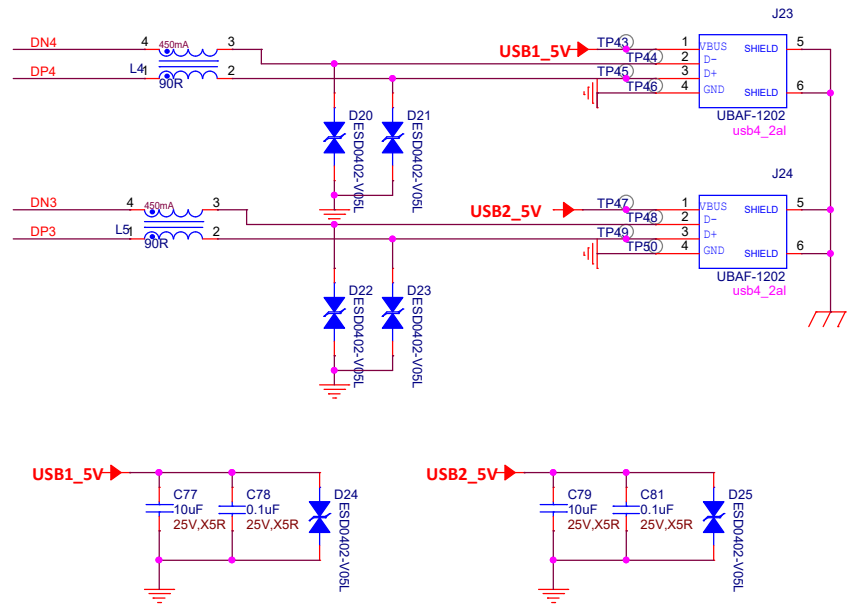
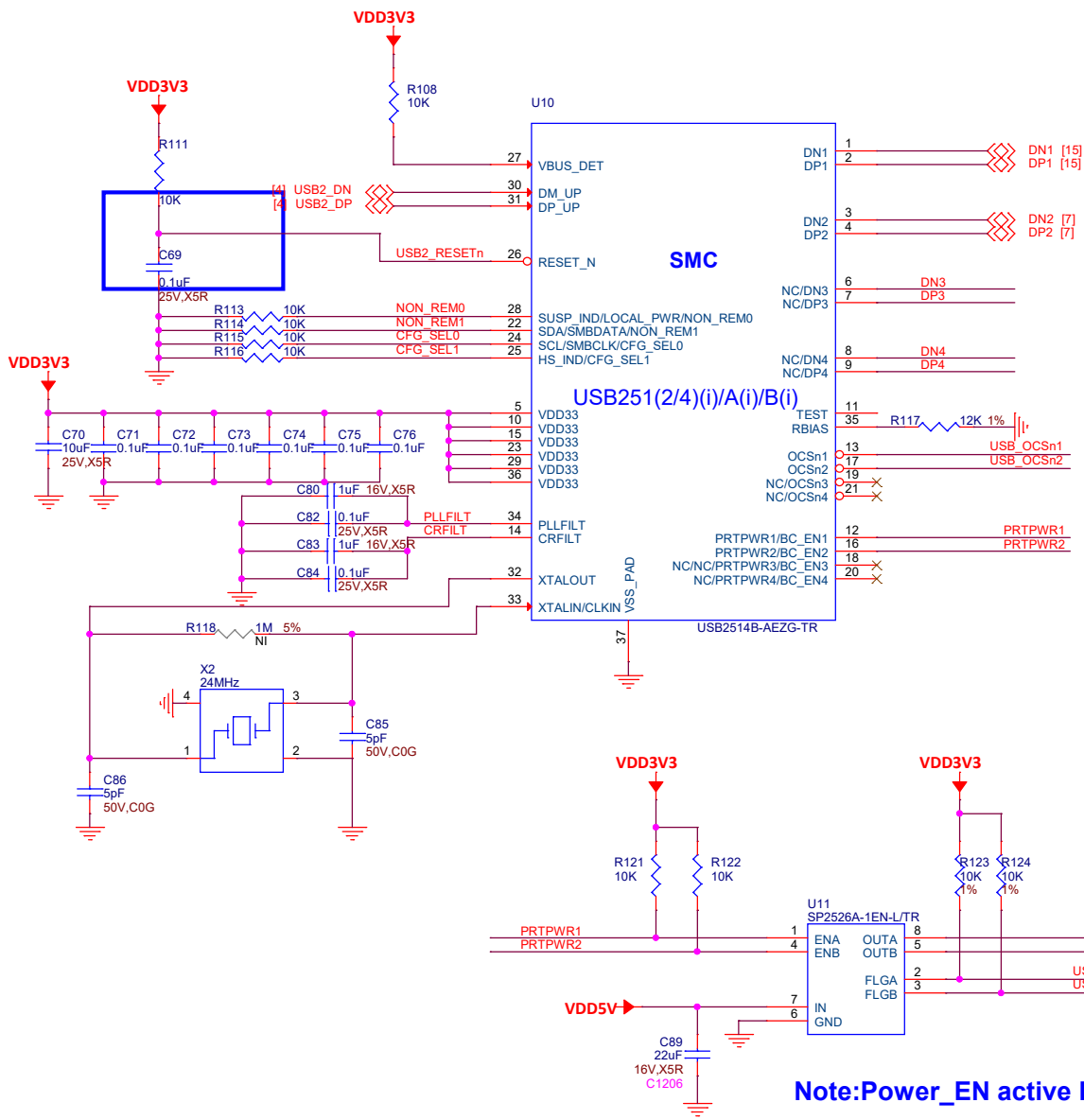


Title:		<Title>	
Size: B	Document Number: <Doc>	Rev: Rev0.0	
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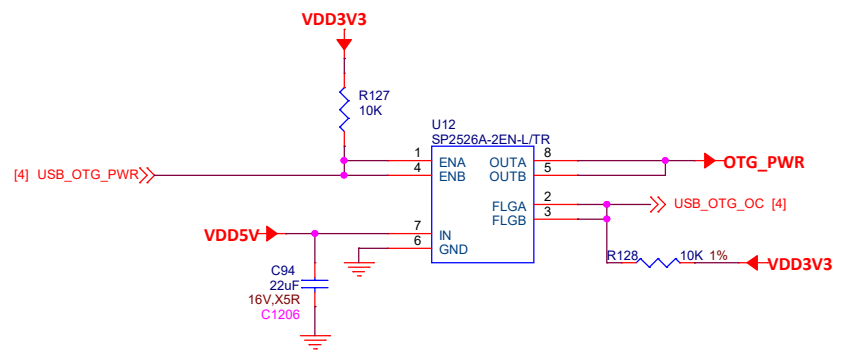
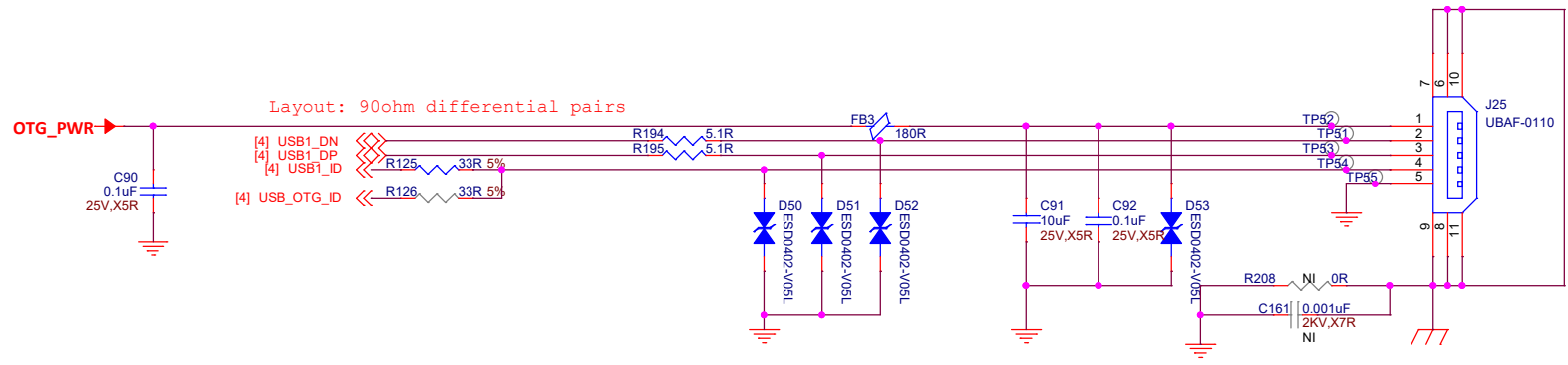
Title:		<Title>	
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USB HOST



Note: Power_EN active Low

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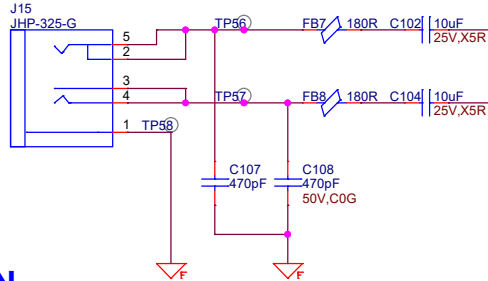


Note: Power_EN active Low

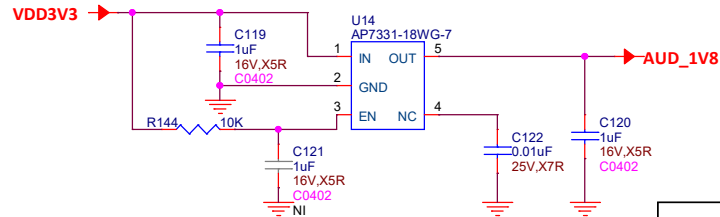
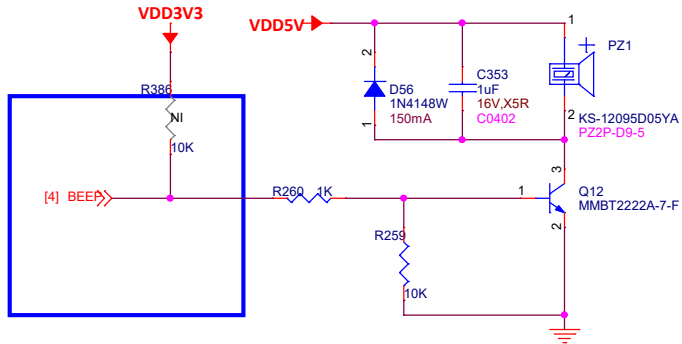
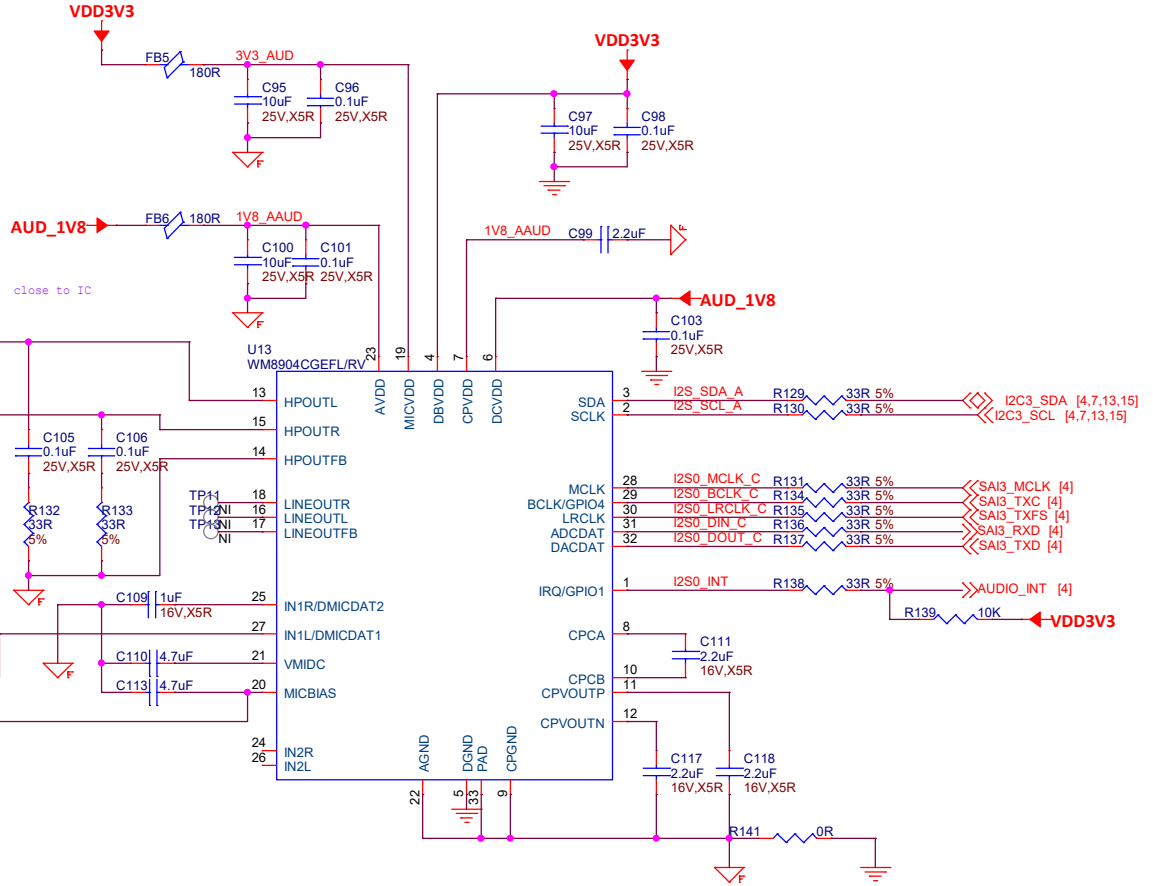
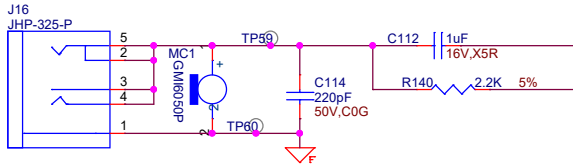
Title: <Title>	
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AUDIO

Phone OUT

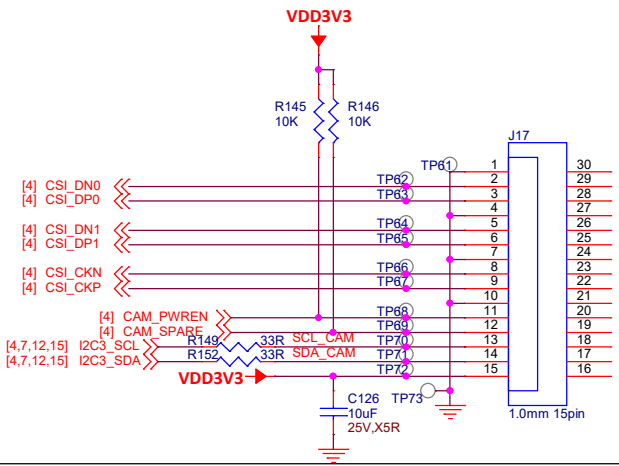


MIC IN

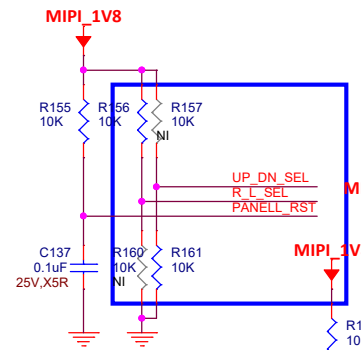
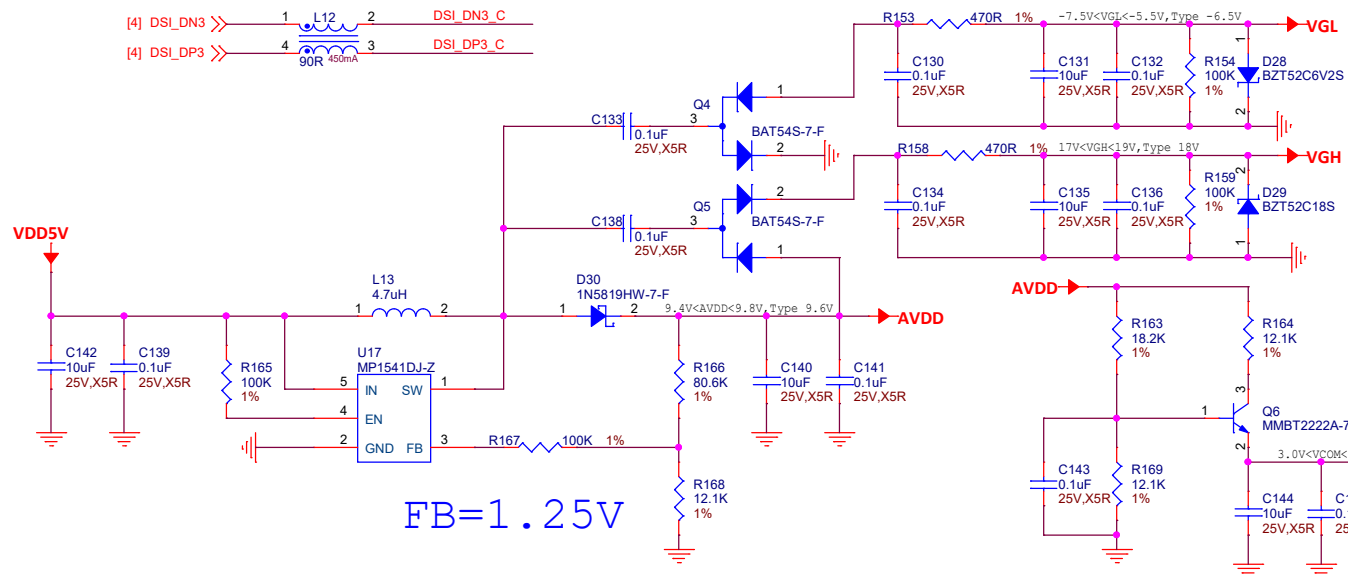
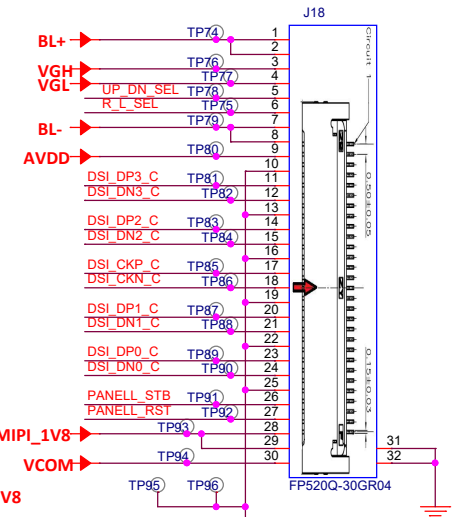
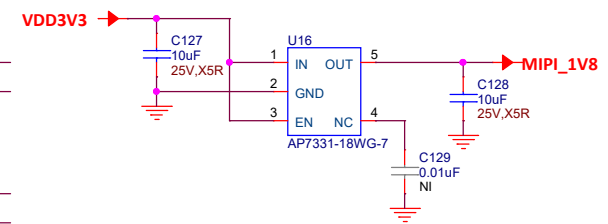
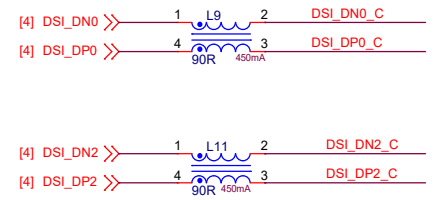
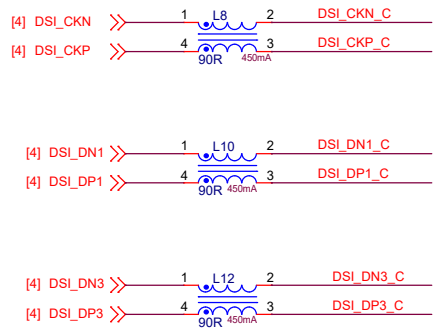
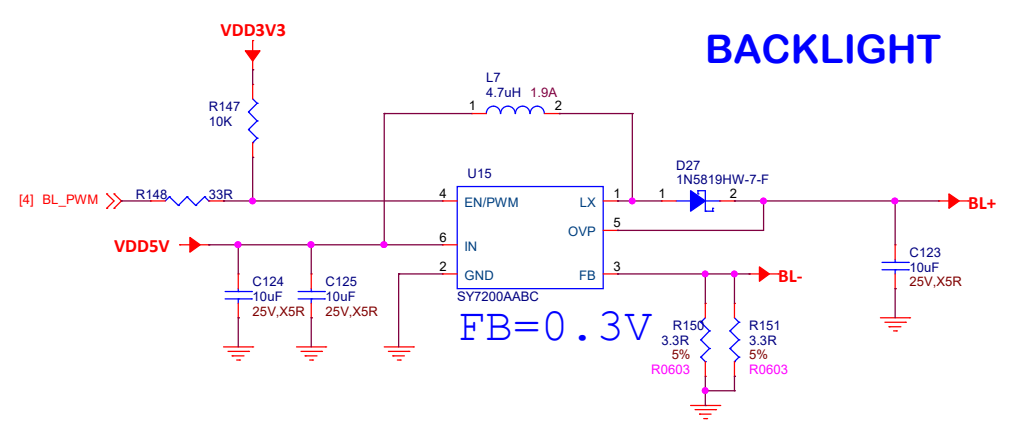


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MIPI CSI



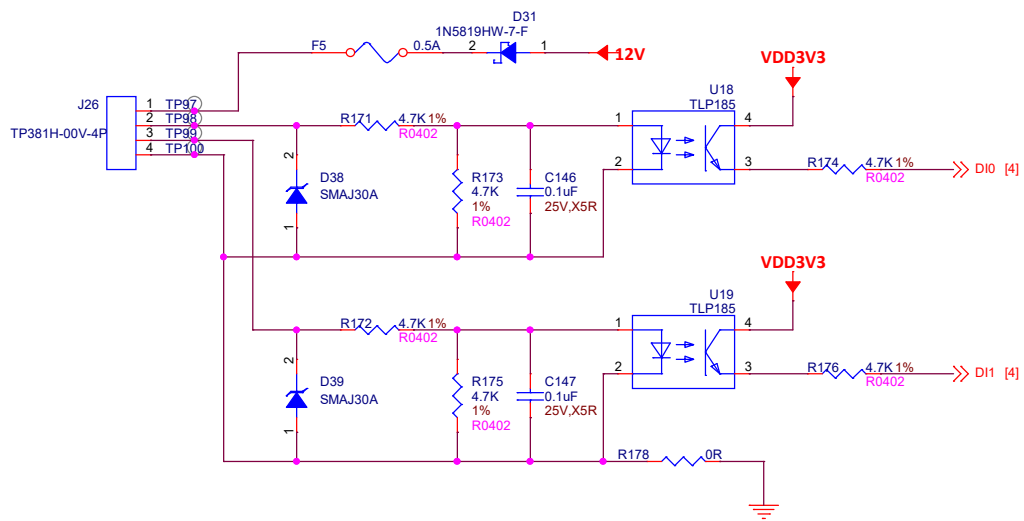
BACKLIGHT



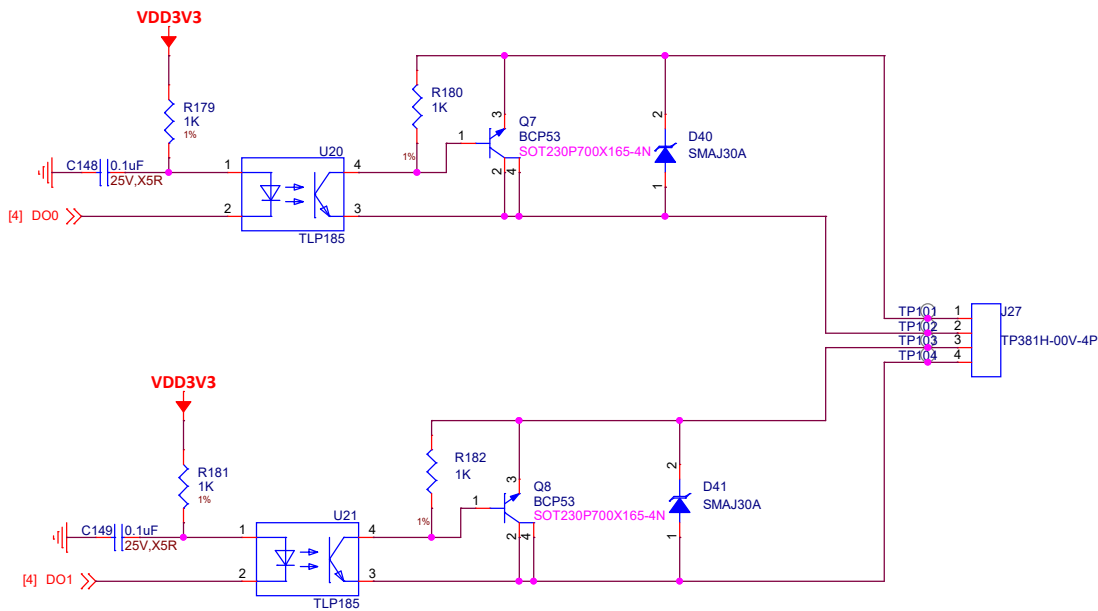
1024*600 LCD

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DI

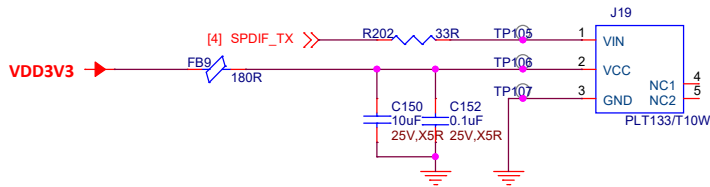


DO

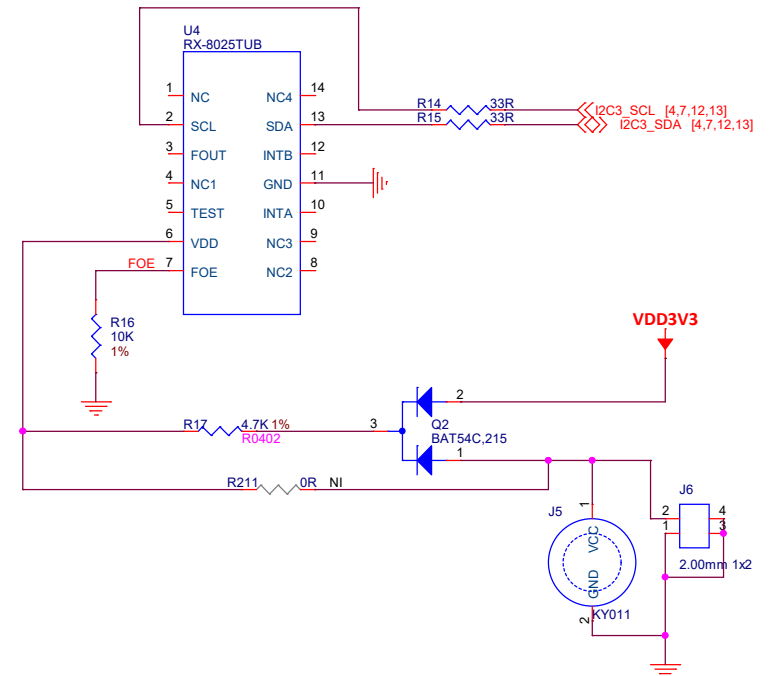


Title:		<Title>	
Size:	Document Number:	Rev:	
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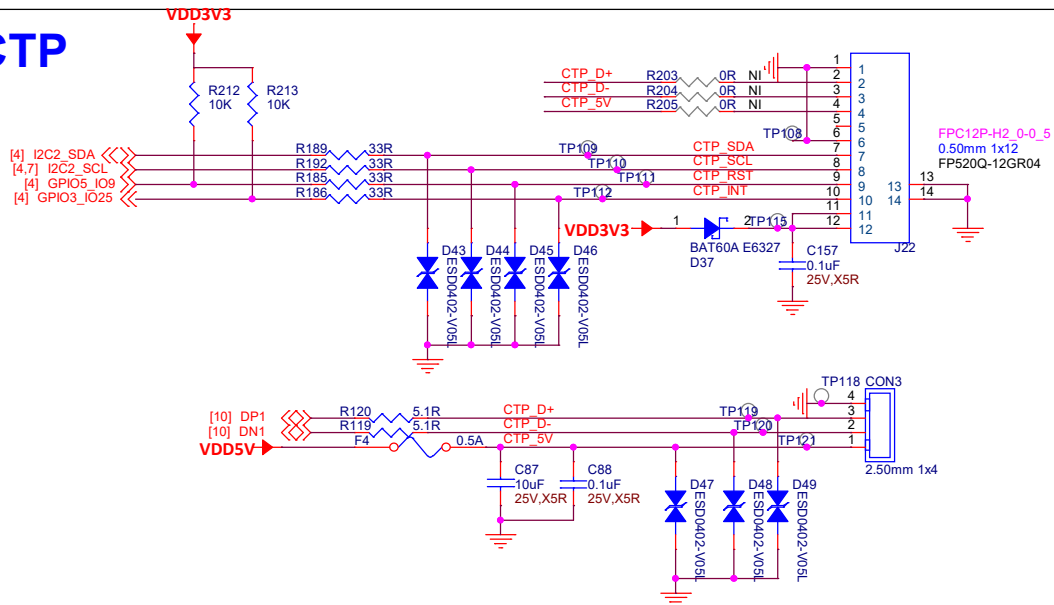
SPDIF



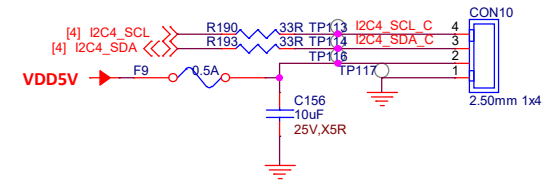
RTC



CTP



I2C



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